REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5-20 are presently pending in this application, Claims 5-18 having been withdrawn from further consideration by the Examiner, Claim 1 having been amended by the present amendment.

In the outstanding Office Action, Claims 1 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Strandberg et al. (U.S. Patent 6,323,435) in view of Tsukada et al. (U.S. Patent 6,809,415) and Cooray (U.S. Patent 6,749,927); Claims 2 and 3 were rejected under 35 U.S.C. §103(a) as being unpatentable over the modified board of Strandberg et al. in view of Westbrook et al. (U.S. Patent 6,203,967); and claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over the modified board of Strandberg et al. in view of Lykins et al. (U.S. Patent 6,440,641).

Claim 1 has been amended. This amendment is believed to find support in the specification, claims and/or drawings as originally filed, for example, the specification, page 15, line 9, to page 16, line 11, and page 60, line 15, to page 61, line 18, as well as Figures 30 and 31, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the rejection based on the cited reference, a brief review of Claim 1 as currently amended is believed to be helpful. Claim 1 is directed to a multilayer printed wiring board and recites: "a core substrate having a first surface and a second surface on an opposite side of the first surface; a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively, and comprising one of a power source conductor and a grounding conductor; a plurality of interlayer insulation layers formed

on the first conductive layers, respectively, and the core substrate; a plurality of second conductive layers formed on the interlayer insulation layers, respectively; and a signal through hole formed though the core substrate, the first conductive layers and the interlayer insulating layers, wherein the first conductive layers on the core substrate have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers, and each of the first conductive layers on the core substrate has a side face which disconnects the first conductive layers from the signal through hole and which is tapered such that an angle, Θ, formed by a straight line connecting the top end and bottom end of the side face of each of the first conductive layers and a horizontal face of the core substrate satisfies $2.8 < \tan \Theta < 55$."

It is respectfully submitted that none of Strandberg et al., Tsukada et al., Cooray and Lykins et al. teaches or suggests "a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively, and comprising one of a power source conductor and a grounding conductor ...; and a signal through hole formed though the core substrate, the first conductive layers and the interlayer insulating layers, wherein the first conductive layers on the core substrate have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers, and each of the first conductive layers on the core substrate has a side face which disconnects the first conductive layers from the signal through hole and which is tapered such that an angle, Θ, formed by a straight line connecting the top end and bottom end of the side face of each of the first conductive layers and a horizontal face of the core substrate satisfies $2.8 < \tan \Theta < 55$" as recited in amended Claim 1.

More specifically, Strandberg et al. states that the conductive traces 14a , 14 b in Figs. 1-5 have a thickness in the range of 20 μm to 30 μm[1] and that the wiring pattern 114a on the substrate 112 has a thickness in the range of 10 μm to 20 μm,[2] thus making the conductive pattern on the surface of the substrate much thinner with much less filler to provide a lower dielectric constant to the structure and thus a lower impedance.[3] As such, it is believed that Strandberg teaches away from making the thickness of the conductive layers on the core substrate larger than the thickness of the conductive layers on the interlayer insulation layer. Furthermore, Strandberg et al. simply shows a junction 17 (*i.e.*, a through hole conductive structure) connected to both inner conductive layers 18a, 18b and outer conductive layers 26a, 26b and does not disclose inner conductive layers with tapered side faces disconnected from the junction 17.

Tsukada et al. merely describes providing superior adhesion between a substrate and a conductor pattern by forming a conductor pattern with a trapezoidal cross-section and a solder resist coated on the conductor pattern, Cooray shows a core substrate, wiring layers 8 formed inside the core substrate, fine wiring layers 7 formed on both sides of the core substrate and a through hole 5 connecting the fine wiring layers 7 on both sides of the core substrate, and Westbrook et al. describes providing a grounding plane layer (a patterned conductive layer or a metal clad conductive layer) on the surface of a high density interconnect wiring board, *not a core substrate*. Lykins et al. is cited simply for the copper foil and plated films of the first conductive layers.

Thus, Strandberg et al., Tsukada et al., Cooray and Lykins et al. are not believed to teach or suggest the first conductive layers as recited in amended Claim 1, and the structure

[1] See Strandberg, column 8, lines 4-9.
[2] See id., column 9, lines 16-23.
[3] See Strandberg, column 9, lines 23-34.

recited in Claim 1 is also believed to be distinguishable from Strandberg et al., Tsukada et al., Cooray and Lykins et al.

Because none of Strandberg et al., Tsukada et al., Cooray and Lykins et al. discloses the first conductive layer structure as recited in Claim 1, their teachings even in combination are not believed to render the multilayer printed wiring board recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2, 3, 19 and 20 depend from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2, 3, 19 and 20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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